IN THE CLAIMS

Each claim of the present application is set forth below with a parenthetical notation immediately following the claim number indicating the current claim status. The Examiner's entry of the claim amendments, as shown in marked-up form, under Section 1.116 is respectfully requested.

1. (CURRENTLY AMENDED) A fusible link device disposed on a semiconductor substrate, comprising:

a first substantially linear material layer having a first sheet resistance and defining first and second terminals at opposing ends thereof, the terminals having a substantially similar triangular shape and size;

a second material layer coextensive with and overlying the first material layer throughout a length bounded by the first and the second terminals, the second material layer having a second sheet resistance less than the first sheet resistance;

wherein the fusible link is programmable to an opened state in which an opening is formed in the first and the second material layers; and

wherein in a closed state the first and the second material layers provide a current path therethrough.

2. (ORIGINAL) The fusible link of claim 1 wherein a material of the first material layer comprises doped polysilicon.

3. (ORIGINAL) The fusible link of claim 1 wherein a material of the second material layer comprises a metal silicide.

4. (ORIGINAL) The fusible link of claim 1 wherein a material of the second material layer is selected from among cobalt silicide, titanium silicide, tungsten silicide, molybdenum silicide and nickel silicide.

5. (PREVIOUSLY PRESENTED) The fusible link of claim 1 operative with a current source for controllably passing a current between the first and the second terminals through the doped polysilicon layer and the silicide layer for creating the openings therein.

6. (ORIGINAL) The fusible link of claim 5 wherein the current is about 25 mA at about 3.3 V.

7. (ORIGINAL) The fusible link of claim 5 wherein the current source comprises a voltage source and a controllable switch connected in series thereto, wherein the switch is operative to a closed state in which current is supplied to the fusible link.

8. (ORIGINAL) The fusible link of claim 1 wherein a data bit is represented by the opened state and the closed state.

9. (CURRENTLY AMENDED) A semiconductor integrated circuit comprising:

a substrate;

doped regions within the substrate, wherein the doped regions form active devices;

a fuse structure comprising:

a first substantially linear material layer having a first sheet resistance having first and second terminals at opposing ends thereof, the terminals having a substantially similar triangular shape and size;

a second material layer coextensive with and overlying the first material layer, the second material layer having a second sheet resistance less than the first sheet resistance;

wherein the fuse structure is programmable to an opened state in which an opening is formed in the first and the second material layers; and

wherein in a closed state the first and the second material layers are intact.

10. (ORIGINAL) The semiconductor integrated circuit of claim 9 further comprising a MOSFET active device formed from doped regions within the substrate, wherein the MOSFET further comprises a gate, and wherein a material of the gate comprises the first material layer.

11. (ORIGINAL) The semiconductor device of claim 9 further comprising isolation regions disposed between certain active devices, wherein the fuse structure is disposed over an isolation region.

12. (ORIGINAL) The semiconductor device of claim 11 wherein a material of the isolation region comprises silicon dioxide.

13. (CURRENTLY AMENDED) A method for forming a fusible link in a semiconductor integrated circuit, comprising:

providing a substrate;

forming a first material layer overlying the substrate, wherein the first material layer has a first sheet resistance; ~~and defines first and second terminal ends thereof;~~

forming a fusible link region and triangularly shaped and similarly sized terminal regions at spaced apart ends of the fusible link region from the first material layer;

forming a second material layer overlying the first material layer of the fusible link region, wherein the second material layer is disposed over the first material layer along a length of the fusible link region and the first and the second terminal regions, and wherein the second material layer has a second sheet resistance, and wherein the second sheet resistance is less than the first sheet resistance; and

causing current to flow through the second material layer, wherein the current produces heat for opening the first and the second material layers to program the fusible link to an opened state.

14. (ORIGINAL) The method of claim 13 wherein the step of forming the first material layer comprises forming a doped polysilicon layer.

15. (ORIGINAL) The method of claim 13 wherein the step of forming the second material layer comprises forming a metal silicide layer.

16. (ORIGINAL) The method of claim 13 wherein a material of the second material layer is selected from among cobalt silicide, titanium silicide, tungsten silicide, molybdenum silicide and nickel silicide.

17. (ORIGINAL) The method of claim 13 wherein the step of forming an opening further comprises passing a current through the doped polysilicon layer and the silicide layer for creating the openings therein.

18. (ORIGINAL) The method of claim 17 wherein the current is about 25 mA at about 3.3 V.

19. (ORIGINAL) The method of claim 13 wherein the opening represents a data bit.

20. (ORIGINAL) The method of claim 13 wherein the semiconductor integrated circuit further comprises active devices, and wherein certain of the active devices comprise a gate, and wherein the step of forming the fusible link region further comprises forming a gate and fusible link region from the first material layer.

21. (ORIGINAL) The method of claim 13 wherein the semiconductor integrated circuit further comprises active devices, and wherein certain of the active devices are separated by

isolation regions, and wherein the step of forming a fusible link region further comprises forming the fusible link region overlying an isolation region.